Relationship of the Units

- Basic unit, latch and F/F (unit 11)
- Simple sequential circuits (unit 12)
  - Registers
  - Counters
- Complex sequential circuits : FSM (finite state machine)
  - Simple one: analysis, Mealy & Moore (unit 13)
  - Complex one:
    - Derive state graph and tables (unit 14)
    - Reduce state graph and tables (unit 15)

Unit 14

Derivation of State Graph and Table

Outline

- Design of a sequence detector
- More complex design problems
- Guidelines for construction of state graphs
- Alphanumeric state graph notation

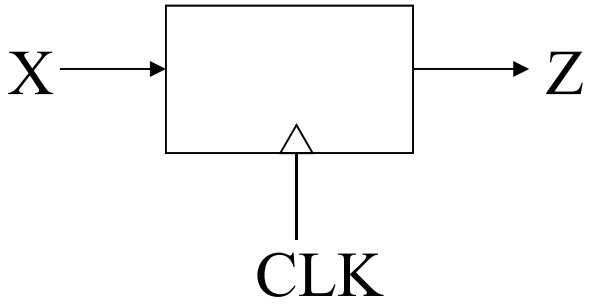
Sequential Circuit Design

- Given a problem statement, to design a sequential circuit
  - 1. Construct a state table or state graph (unit 14)
    - Further simplification (unit 15)
  - 2. Derive F/F input equations and output equations (unit 12)

Design of a Sequence Detector (1/11)

Given problem statement ⇨ state graph
state table

Mealy Machine



Z=1 when detects X=101,
otherwise Z=0

X	=	0	0	1	1	0	1	1	0	0	1	0	1	0	1	0	0
Z	=	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0
(Time	:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15)

Design of a Sequence Detector (2/11)

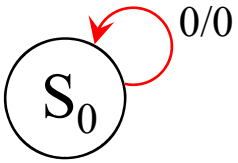
Construction of state graph

Start with a reset state S_0

①

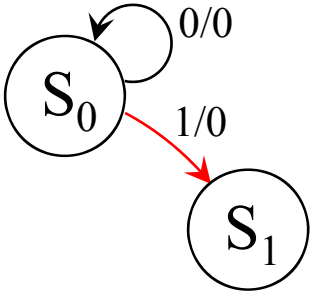
S_0: receices a "0" ⇨ stays at S_0 , Z = 0

0



receives a "1" ⇨ a new state S_1 , Z = 0

01

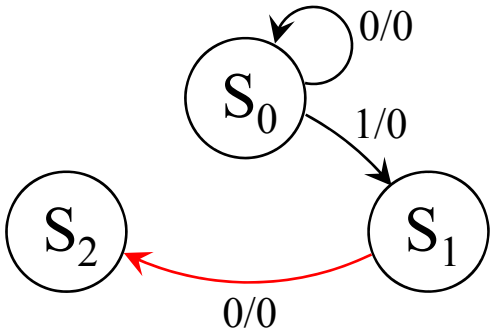


②

Design of a Sequence Detector (3/11)

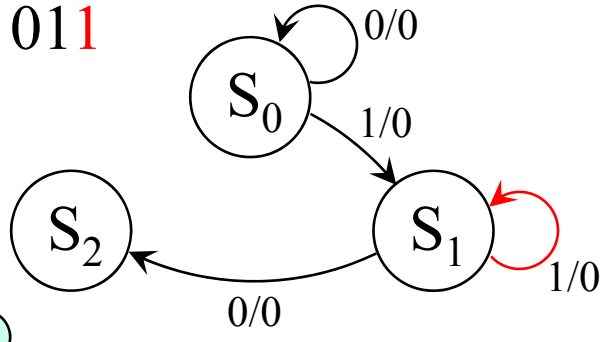
S_1: receices "0" ⇨ S_2 , Z = 0

010



receices "1" ⇨ S_1 , Z = 0

011

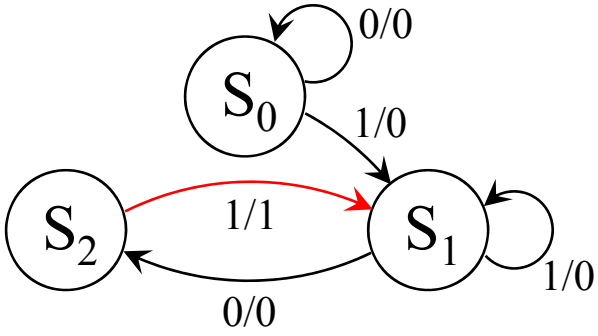


3

S_2: receices "1" ⇨ Z = 0

0101 and goes back to S_1

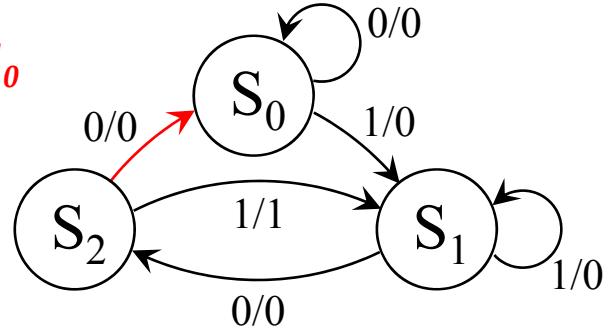
Go back to S_1 since it is also the first 1 in new sequence



receices "0" ⇨ S_0 , Z = 0

0100

Go back to S_0 since 00 is not a part of desired sequence



4

Design of a Sequence Detector (4/11)

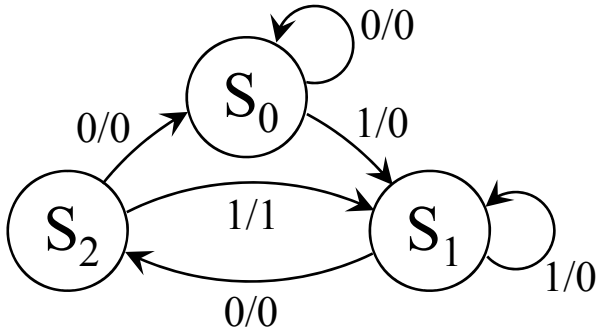
State table

P.S.	N.S. X = 0	N.S. X = 1	Output Z X = 0	Output Z X = 1
S_0	S_0	S_1	0	0
S_1	S_2	S_1	0	0
S_2	S_0	S_1	0	1

State assignment

A F/F can encode 2 states

⇨ 3 states → 2 F/Fs (A, B)



S_0 : AB = 00

S_1 : AB = 01

S_2 : AB = 10

AB	A^+B^+ X = 0	A^+B^+ X = 1	Z X = 0	Z X = 1
00	00	01	0	0
01	10	01	0	0
10	00	01	0	1

Design of a Sequence Detector (5/11)

Choose F/F

Use D F/F

AB	A^+B^+				D_A		D_B	
	X = 0		X = 1		X = 0	X = 1	X = 0	X = 1
00	0	0	0	1	0	0	0	1
01	1	0	0	1	1	0	0	1
10	0	0	0	1	0	0	0	1

K-Map simplification

AB \ X	0	1
00	0	0
01	1	0
11	×	×
10	0	0

$A^+ = D_A = X'B$

AB \ X	0	1
00	0	1
01	0	1
11	×	×
10	0	1

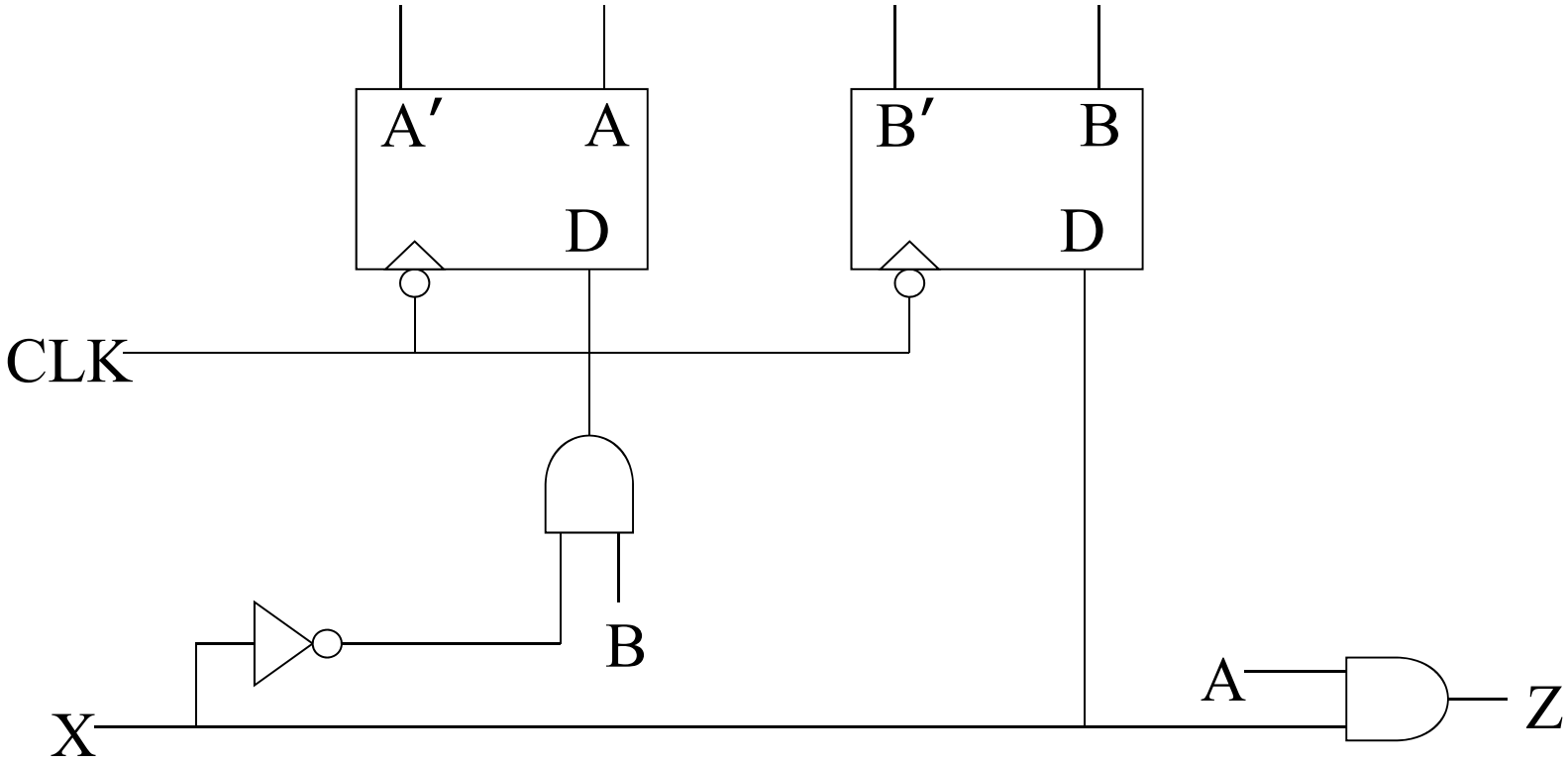
$B^+ = D_B = X$

AB \ X	0	1
00	0	0
01	0	0
11	×	×
10	0	1

$Z = XA$

Design of a Sequence Detector (6/11)

Circuit realization



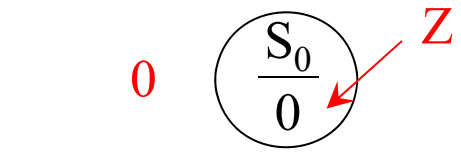
$$A^{+} = D_A = X'B \qquad B^{+} = D_B = X \qquad Z = XA$$

Design of a Sequence Detector (7/11)

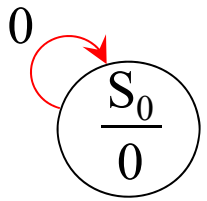
Construction of state graph

Start with a reset state S_0

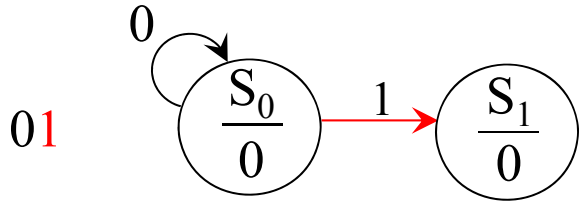
S_0 : $Z = 0$



receives "0" ⇨ S_0



receives "1" ⇨ S_1 (S_1 , $Z = 0$)

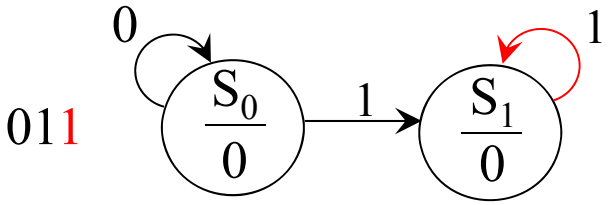


①

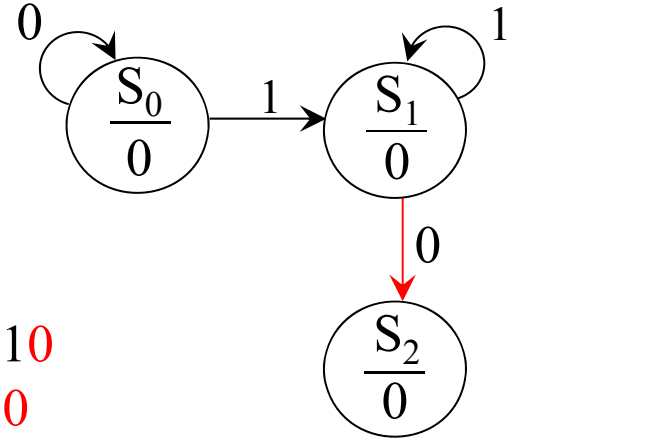
Moore Machine

S_0 : $Z = 0$

receives "1" ⇨ S_1

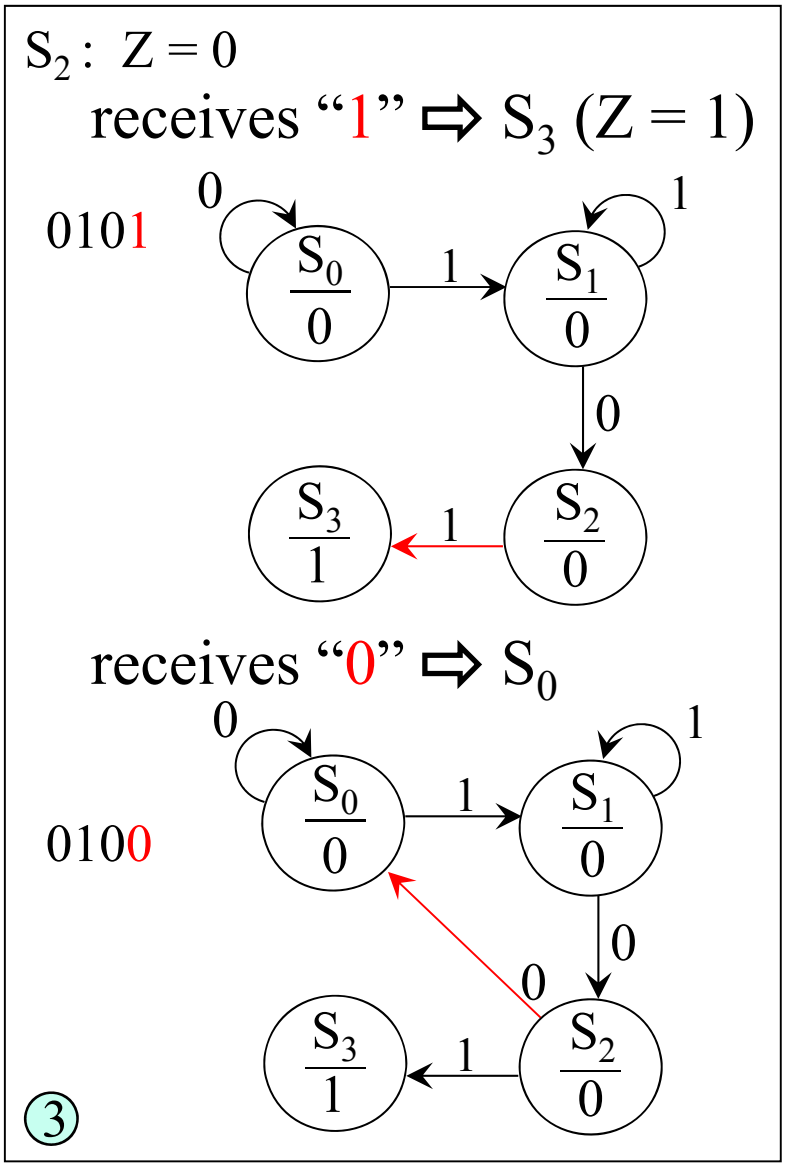


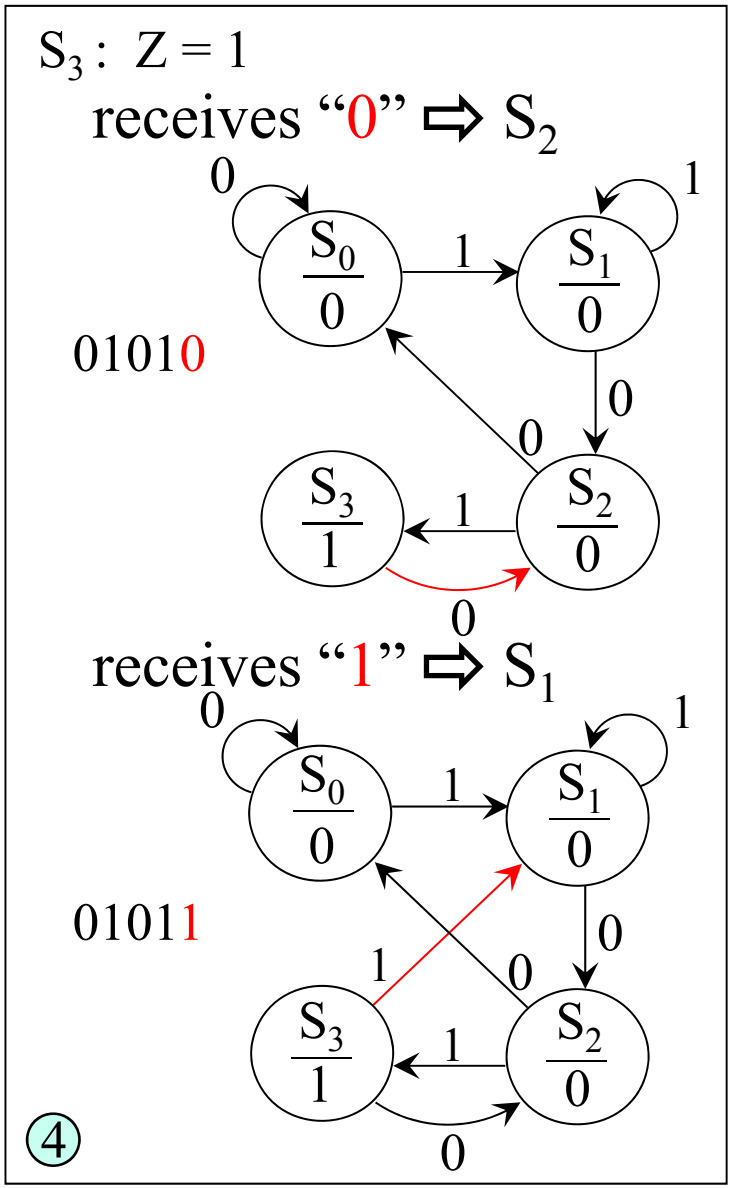
receives "0" ⇨ S_2 ($Z = 0$)



②

Design of a Sequence Detector (8/11)

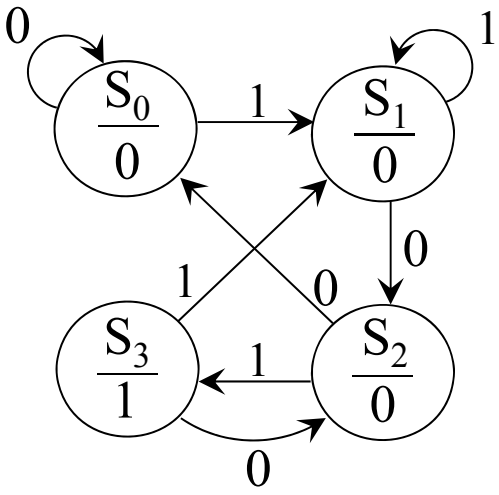




Design of a Sequence Detector (9/11)

State table

P.S.	N.S. X = 0	N.S. X = 1	Present Output Z
S_0	S_0	S_1	0
S_1	S_2	S_1	0
S_2	S_0	S_3	0
S_3	S_2	S_1	1



State assignment

4 states ⇨ 2 F/Fs (A, B)

	AB	A^+B^+ X = 0	A^+B^+ X = 1	Z
S_0	00	00	01	0
S_1	01	11	01	0
S_2	11	00	10	0
S_3	10	11	01	1

Design of a Sequence Detector (10/11)

Choose F/F

Use D F/F

AB	A^+B^+ X = 0		A^+B^+ X = 1		D_A X = 0	D_A X = 1	D_B X = 0	D_B X = 1
00	0	0	0	1	0	0	0	1
01	1	1	0	1	1	0	1	1
11	0	0	1	0	0	1	0	0
10	1	1	0	1	1	0	1	1

K-Map simplification

AB \ X	0	1
00	0	0
01	1	0
11	0	1
10	1	0

AB \ X	0	1
00	0	1
01	1	1
11	0	0
10	1	1

B \ A	0	1
0	0	1
1	0	0

$Z = AB'$

$A^+ = D_A = X'A'B + XAB + X'AB'$ $\quad B^+ = D_B = XA'+A'B+AB'$

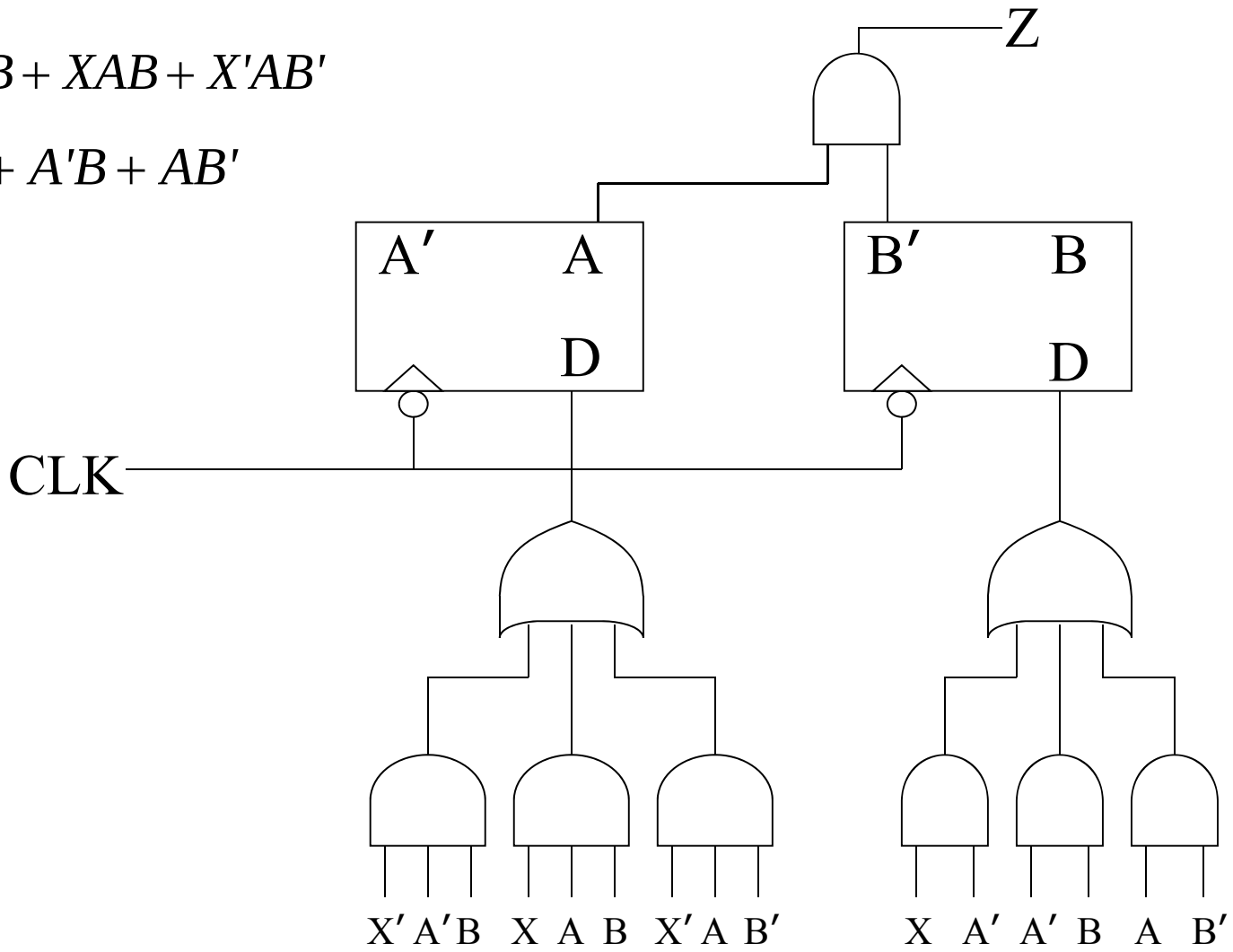
Design of a Sequence Detector (11/11)

Circuit realization

$$A^+ = X'A'B + XAB + X'AB'$$

$$B^+ = XA' + A'B + AB'$$

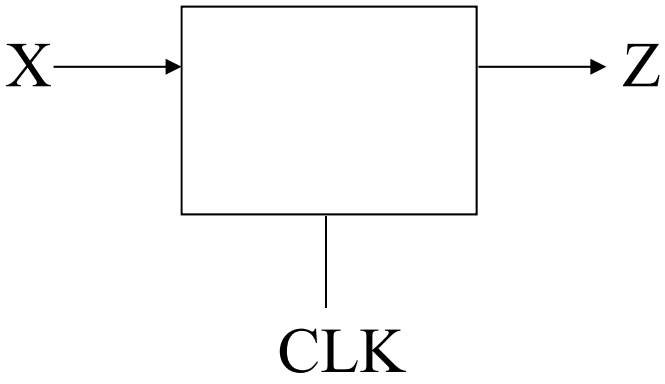
$$Z = AB'$$



More complex Design Problems (1/11)

Mealy Machine

Sequence dectector

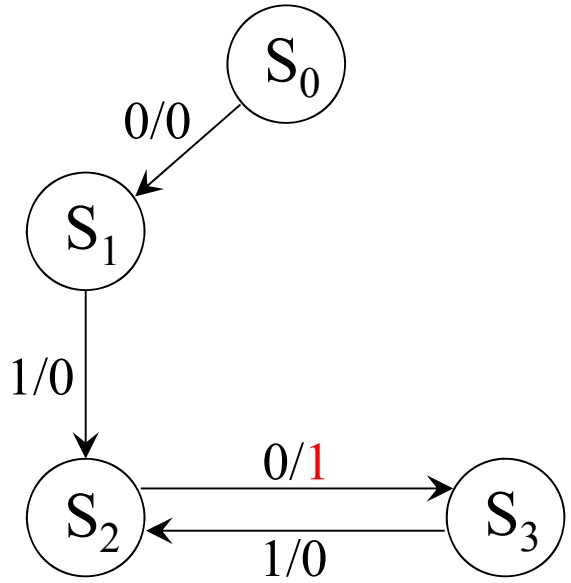


Z=1 when detects X=010 or 1001, otherwise Z=0

X	=	0	0	1	0	1	0	0	1	0	0	0	1	0	0	1	1	0
Z	=	0	0	0	1	0	1	0	1	1	0	0	0	1	0	1	0	0

More complex Design Problems (2/11)

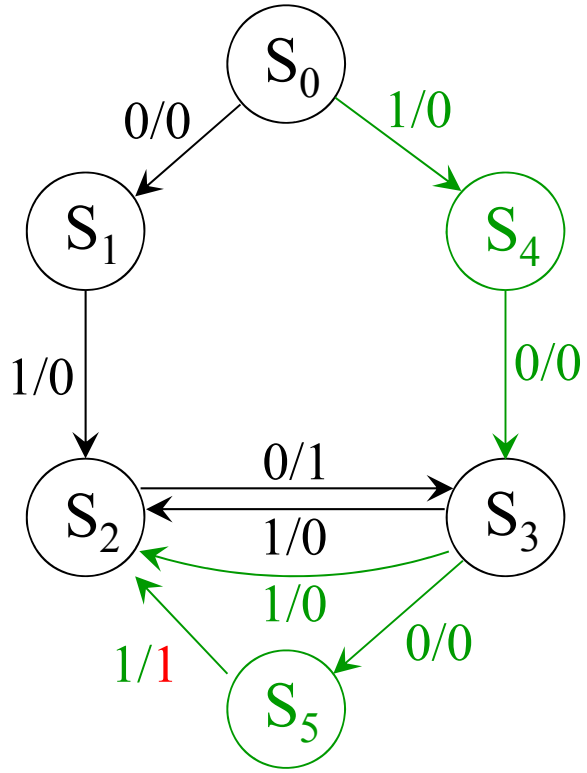
Partial state graph construction for 010



State	Sequence received
S_0	reset
S_1	0
S_2	01
S_3	010

More complex Design Problems (3/11)

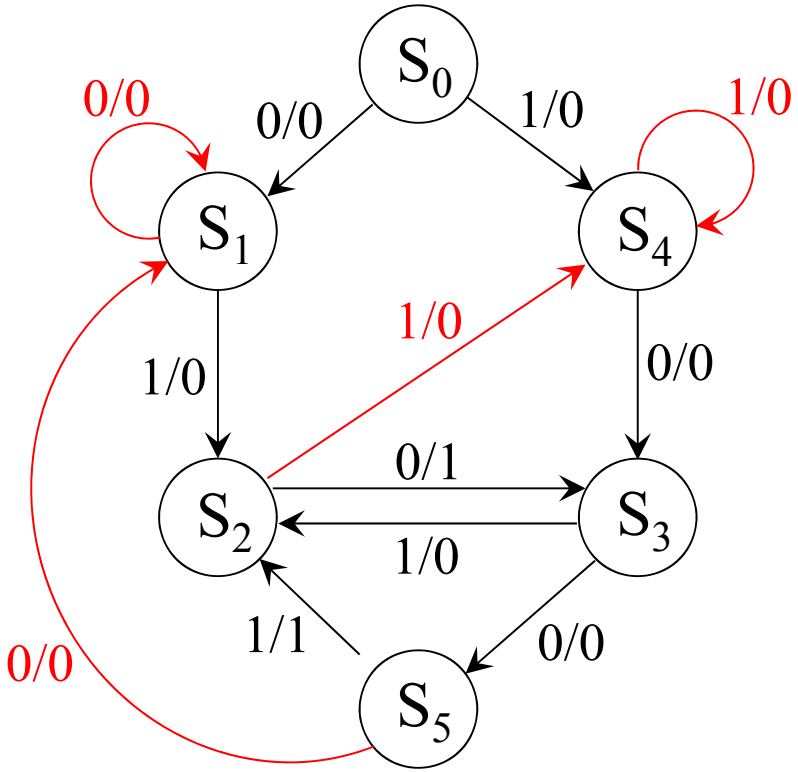
Partial state graph construction for 1001



State	Sequence received
S_0	reset
S_1	0
S_2	01
S_3	010 or 10
S_4	1
S_5	100

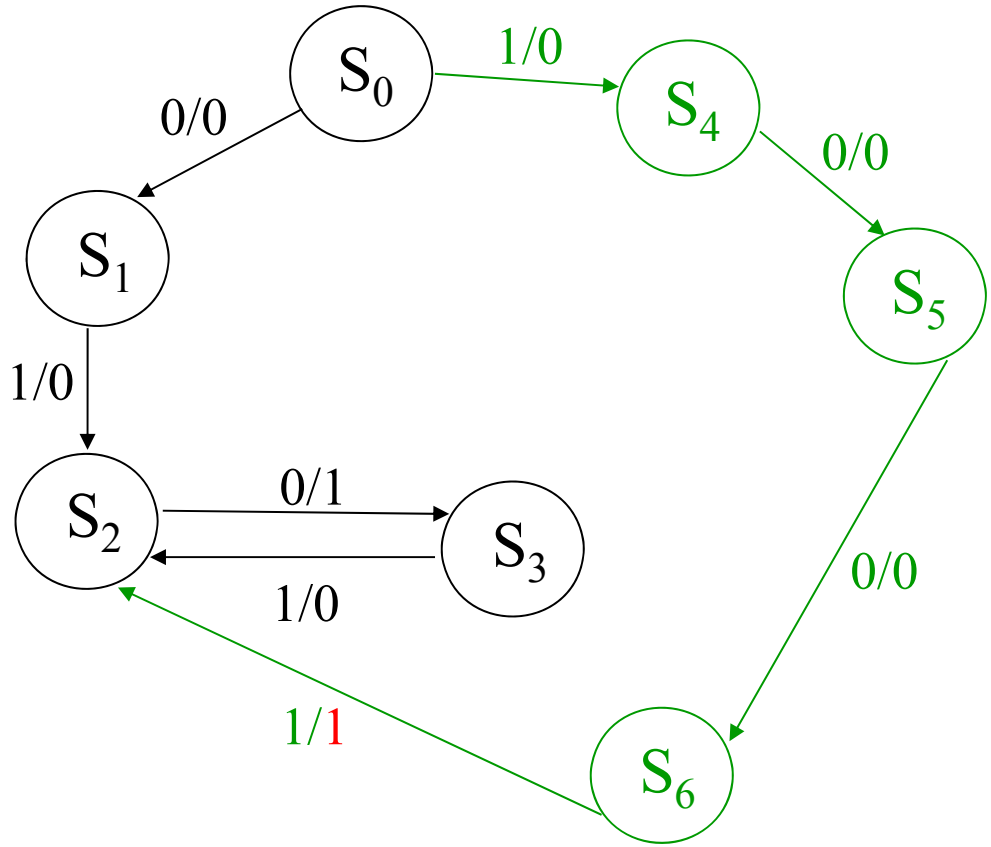
More complex Design Problems (4/11)

Complete state graph



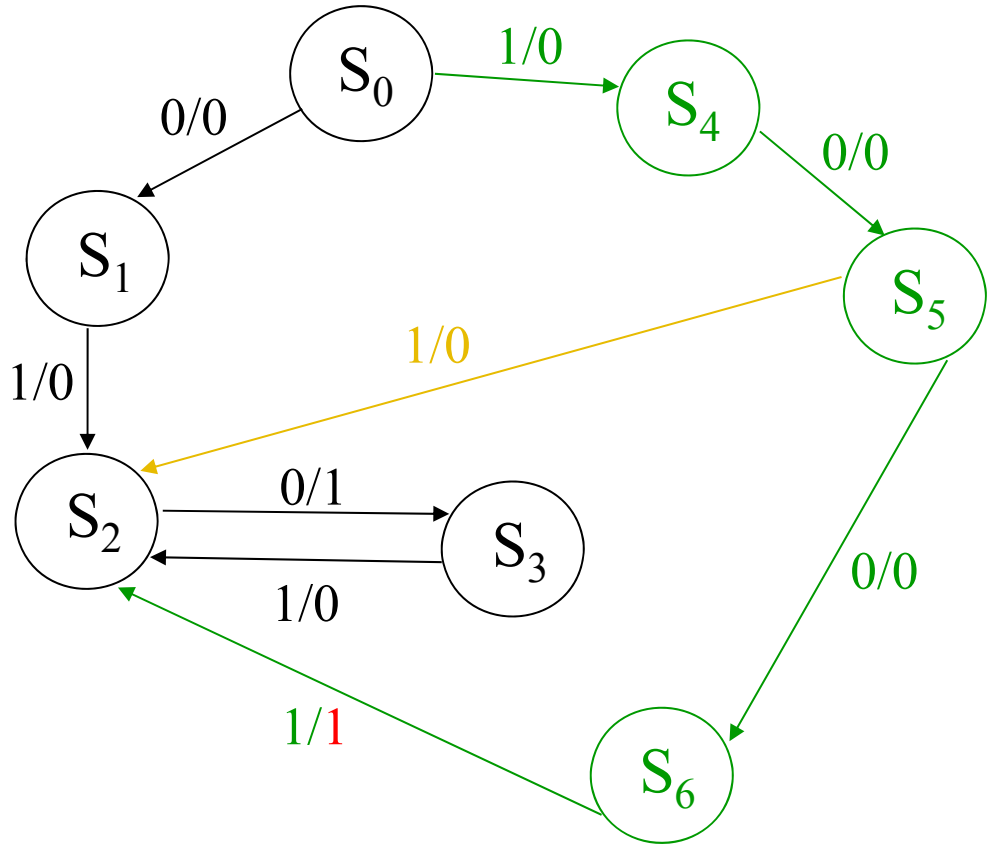
More complex Design Problems (5/11)

If state graph



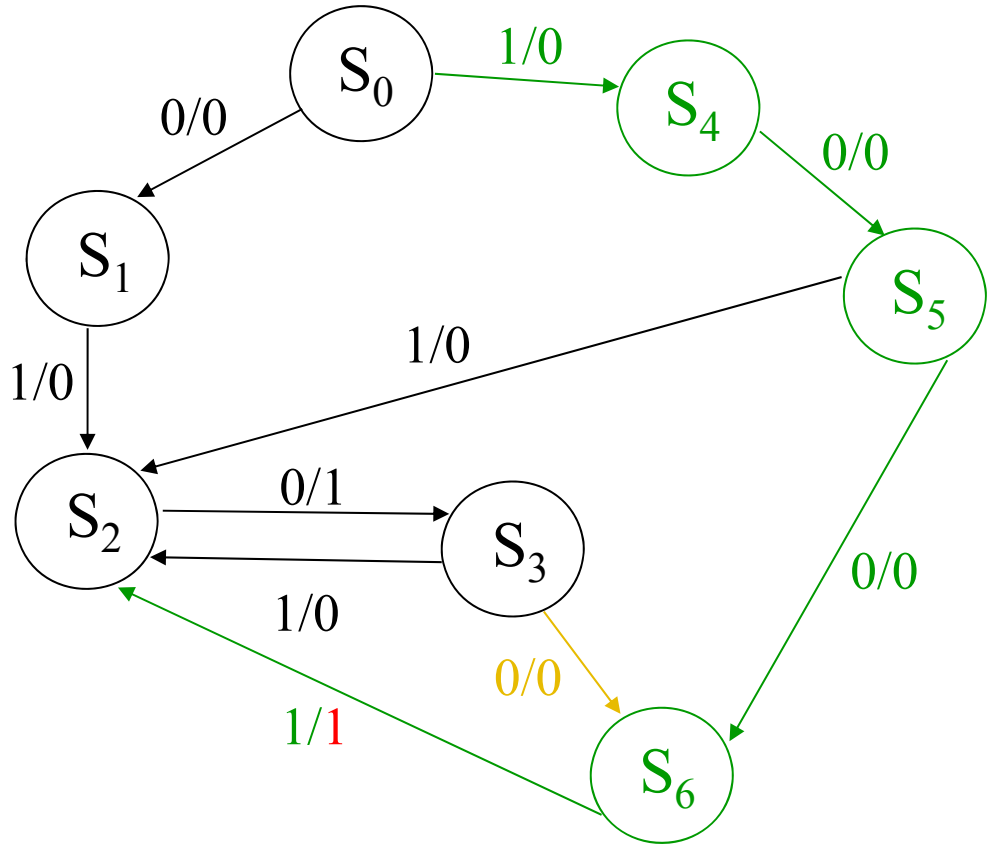
More complex Design Problems (6/11)

Then $S_5 \rightarrow S_2$

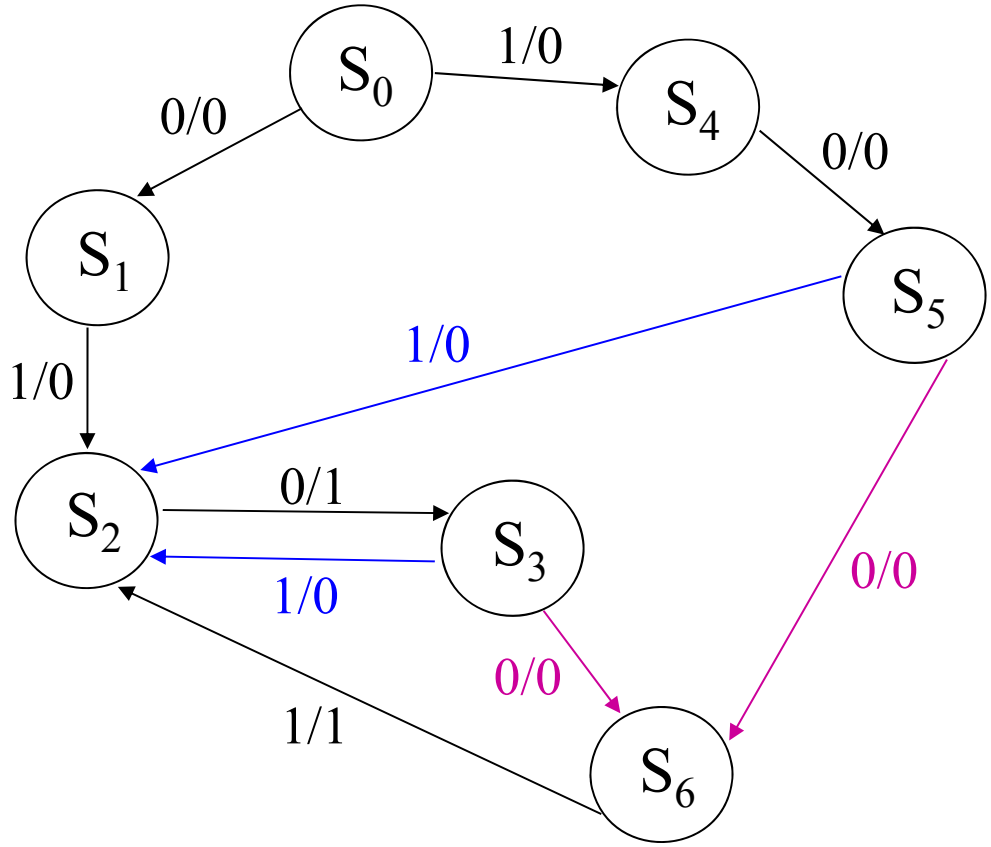


More complex Design Problems (7/11)

Then $S_3 \rightarrow S_6$



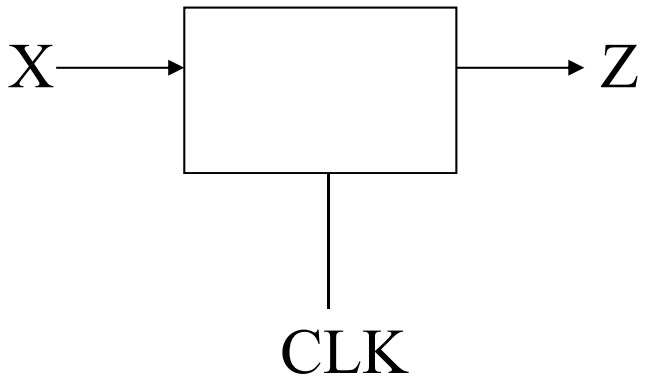
More complex Design Problems (8/11)



S_3, S_5 have the same next states (S_2, S_6) and output 0 under the same input ⇨ $S_3 \equiv S_5$ (equivalent)

More complex Design Problems (9/11)

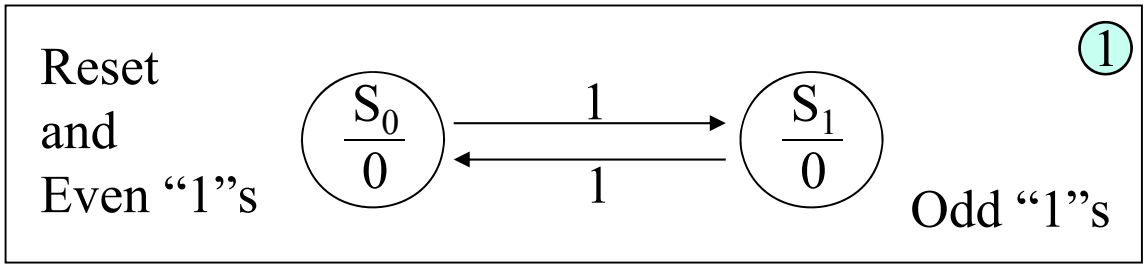
Moore Machine

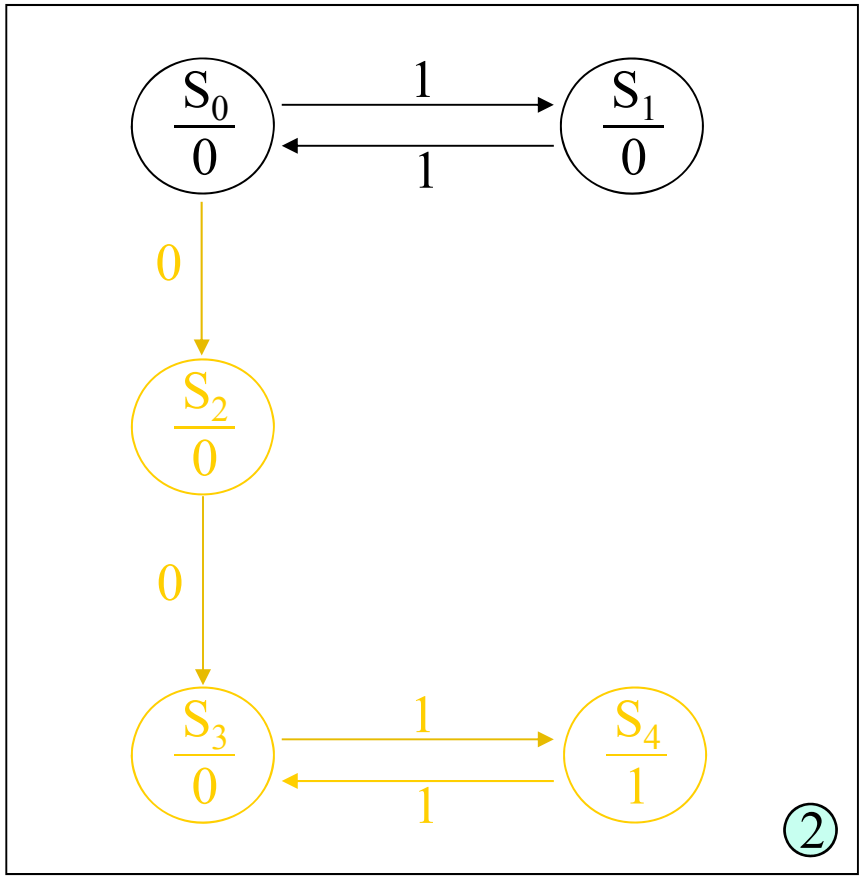


Z = 1 if total number of "1" received is "odd" and at least 2 consecutive "0" received, otherwise, Z = 0

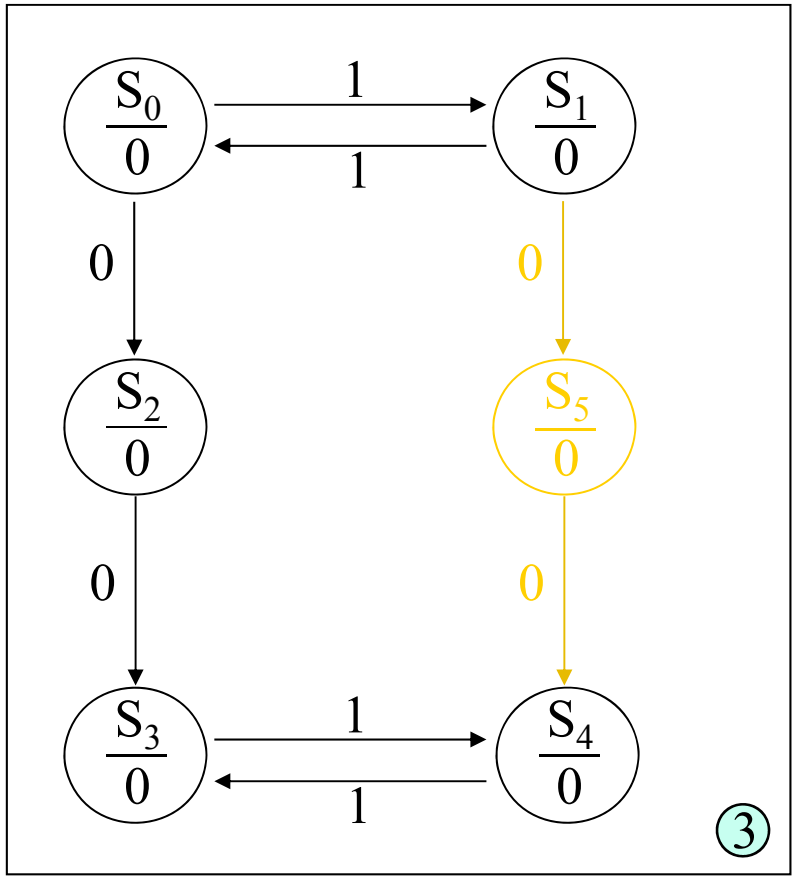
X =		1	0	1	1	0	0	1	1
Z =	(0)	0	0	0	0	0	1	0	1

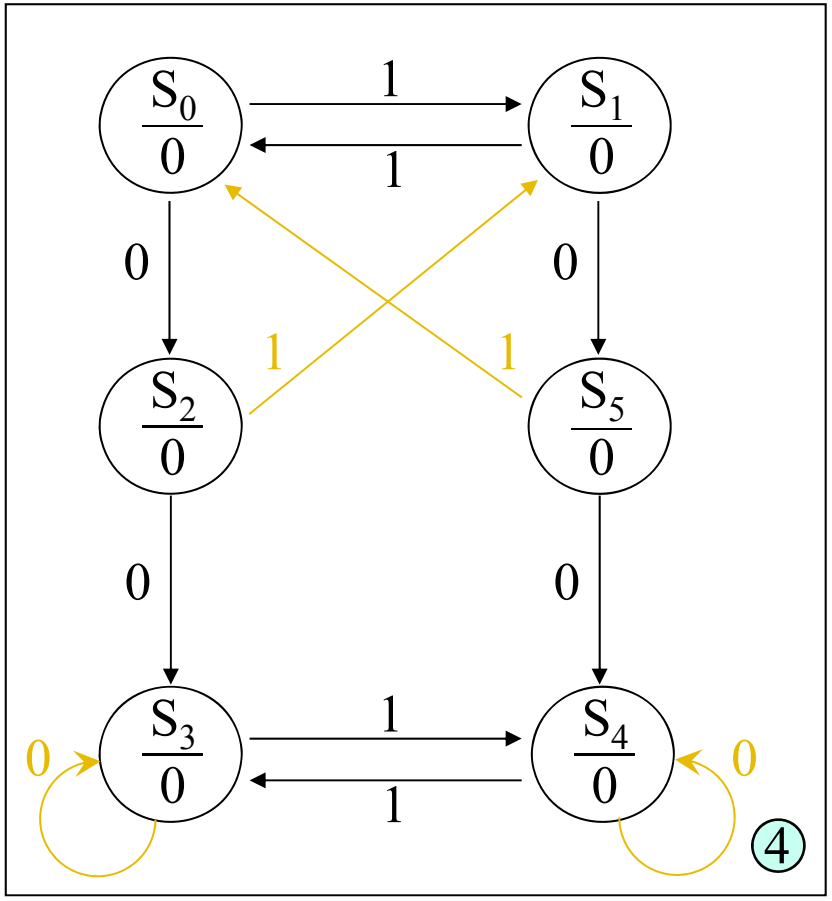
More complex Design Problems (10/11)





More complex Design Problems (11/11)



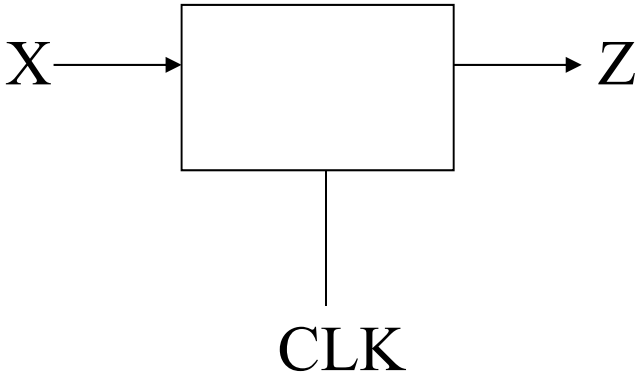


Guidelines for Construction of State Graphs (1/6)

1. Understand the problem by constructing
   sample sequences
2. Determine the reset state
3. Construct a partial graph to obtain "1" output
4. Construct remaining partial graphs to
   obtain "1" output
5. When setting up a new state, see whether
   it can go to an existing state
6. Complete the graph (check all input combinations !!)

Guidelines for Construction of State Graphs (2/6)

Mealy Machine



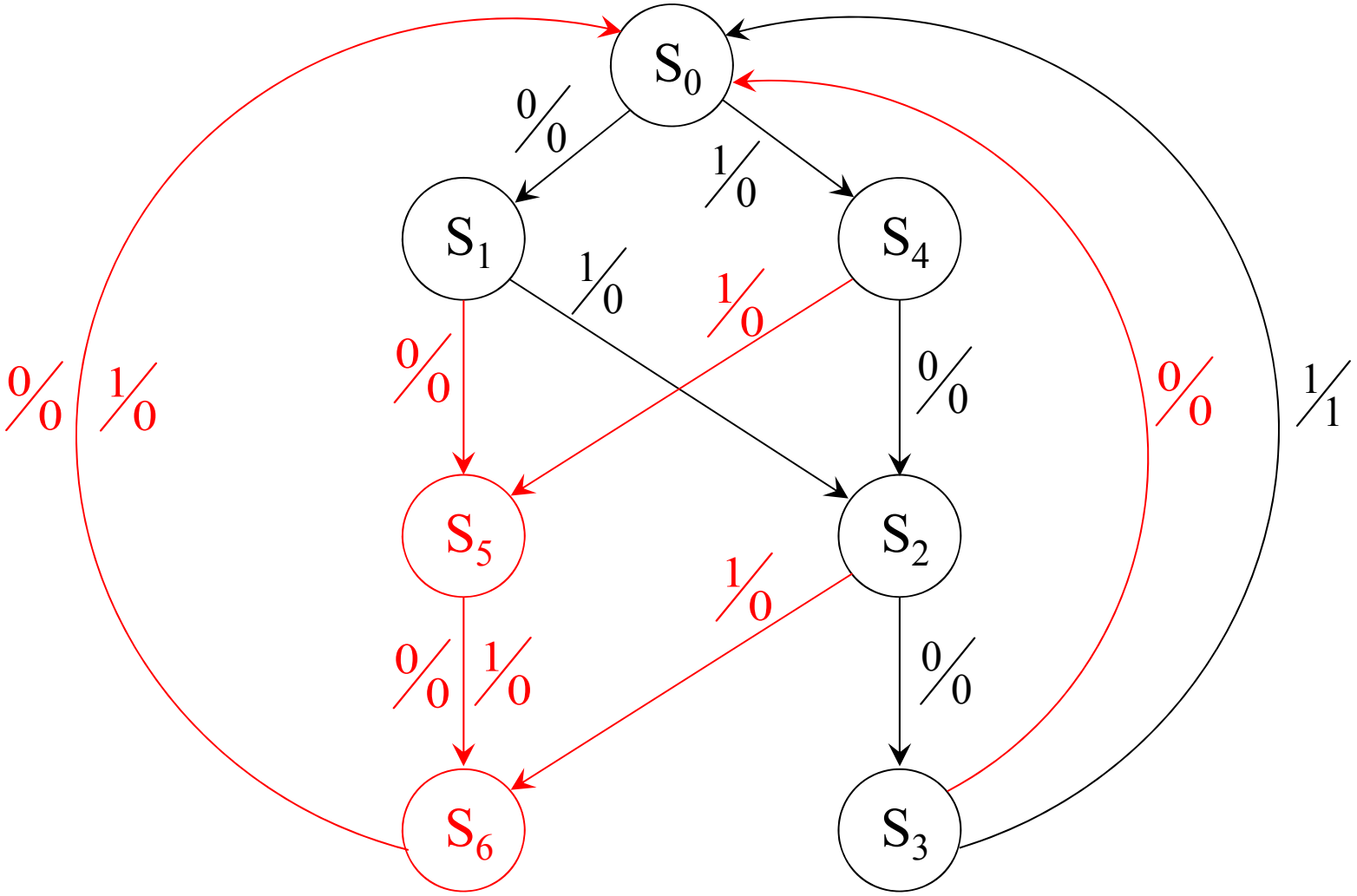
Check 4 consecutive inputs as a group, then reset

Z= 1 when X = 0101 or 1001

X	=	0	1	0	1	0	0	1	0	1	0	0	1	0	1	0	0
Z	=	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

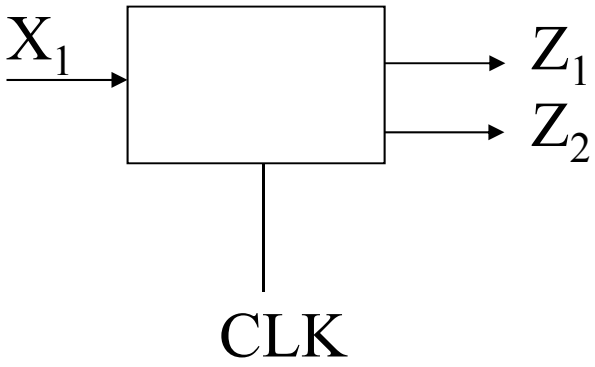
Hint: Z=1 if either 01 or 10 followed by 01

Guidelines for Construction of State Graphs (3/6)



Guidelines for Construction of State Graphs (4/6)

Mealy Machine



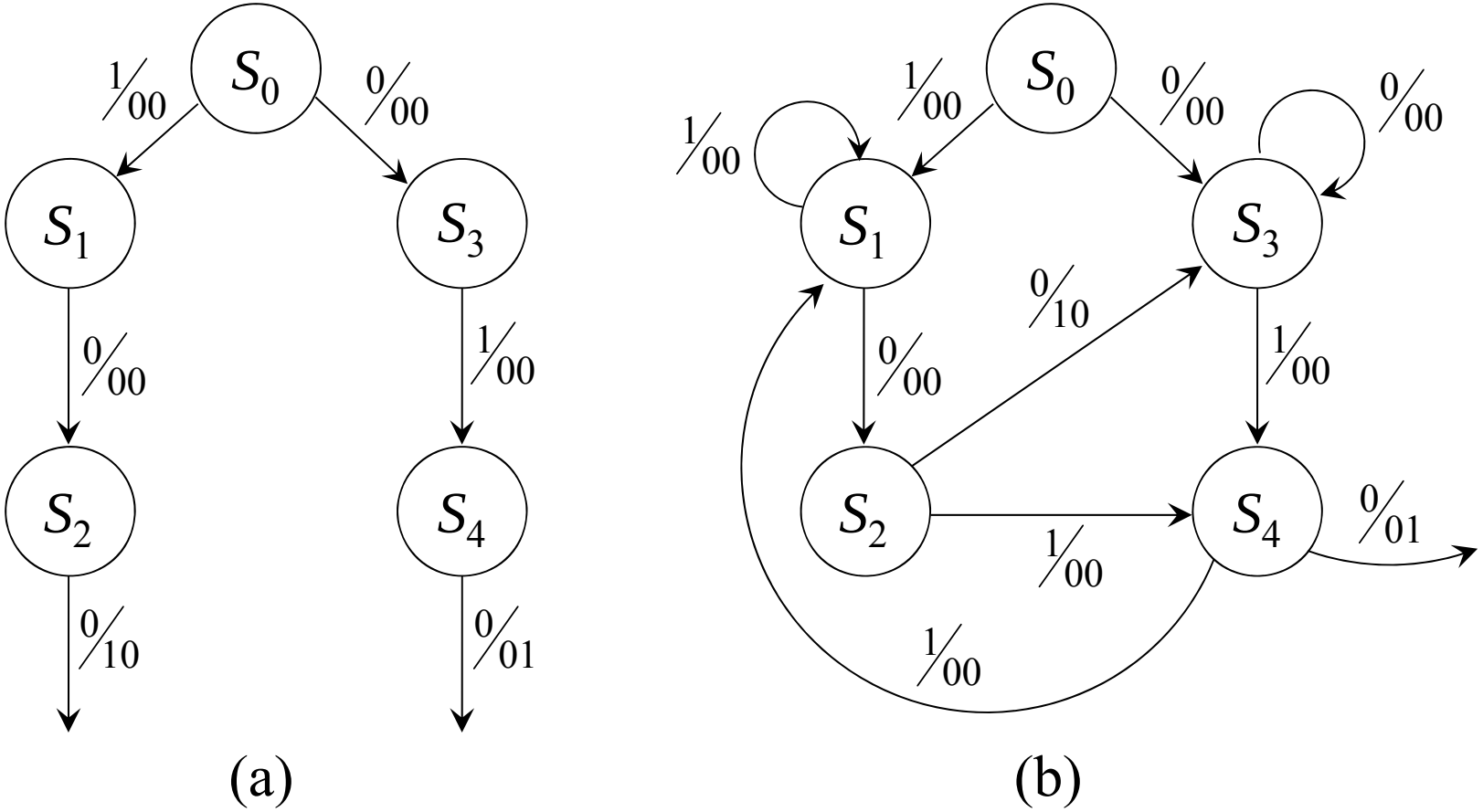
Z_1=1 if sequence 100 occurs & 010 has not occurred

Z_2=1 if sequence 010 occurs,

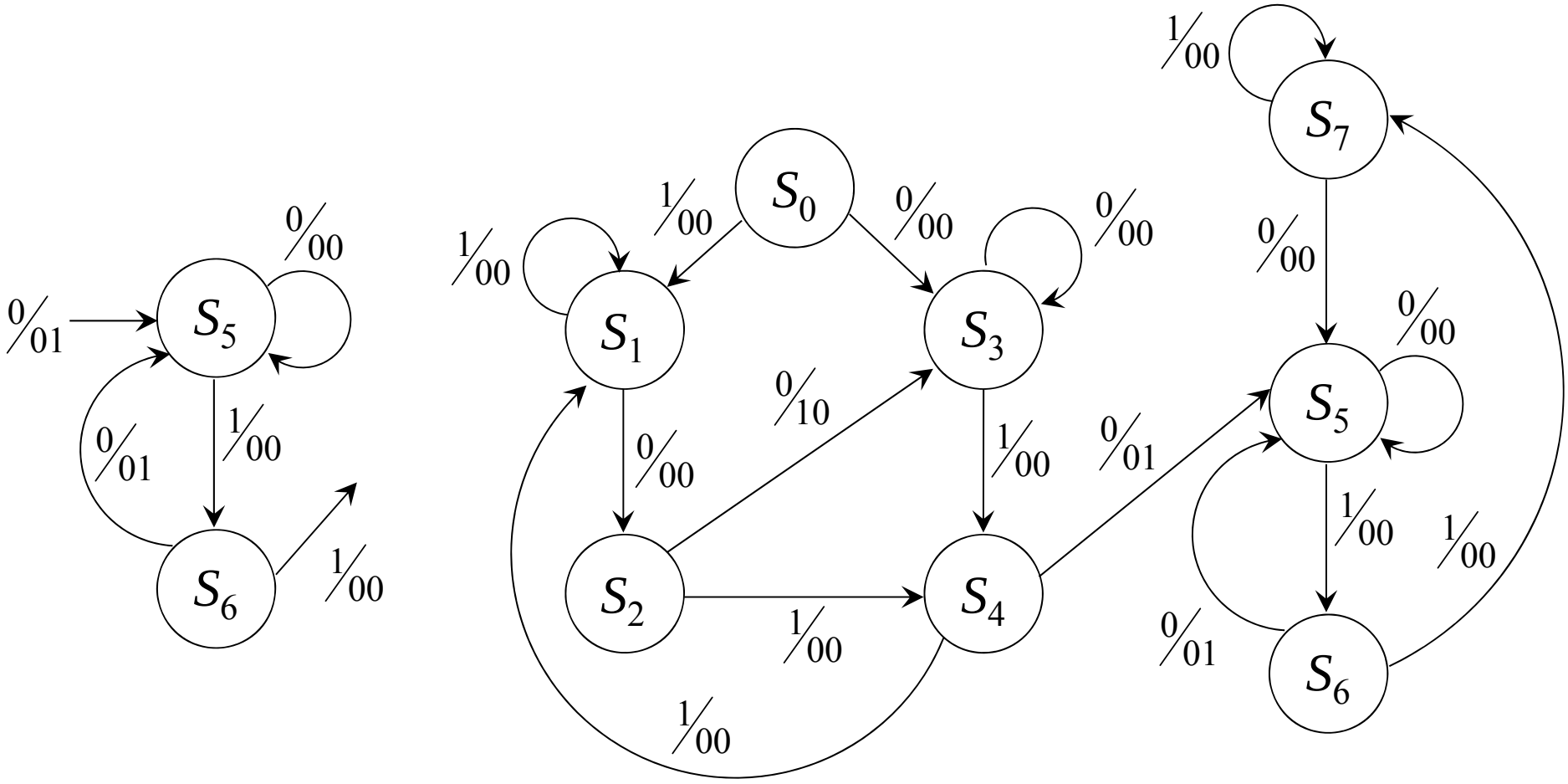
Note once a Z_2 =1, then Z_1 =1 will never occur

X_1 =	1	0	0	1	1	0	0	1	0	1	0	1	0	0	1	0	1	1	0	1	0	0
Z_1 =	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Z_2 =	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	0	0	0	1	0	

Guidelines for Construction of State Graphs (5/6)



Guidelines for Construction of State Graphs (6/6)



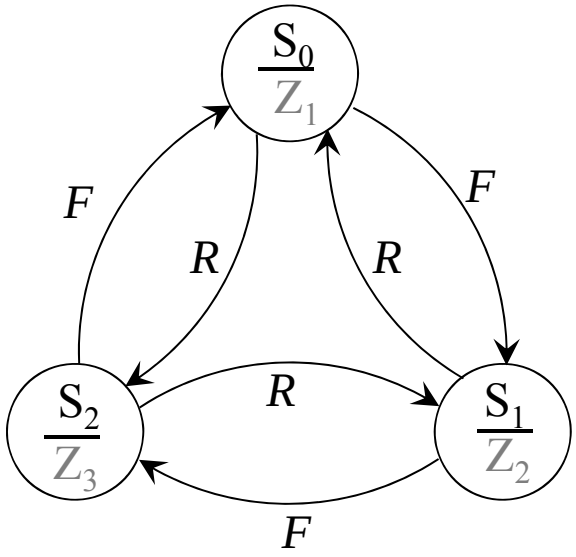
(a) Partial graph for 010

(b) Complete state graph

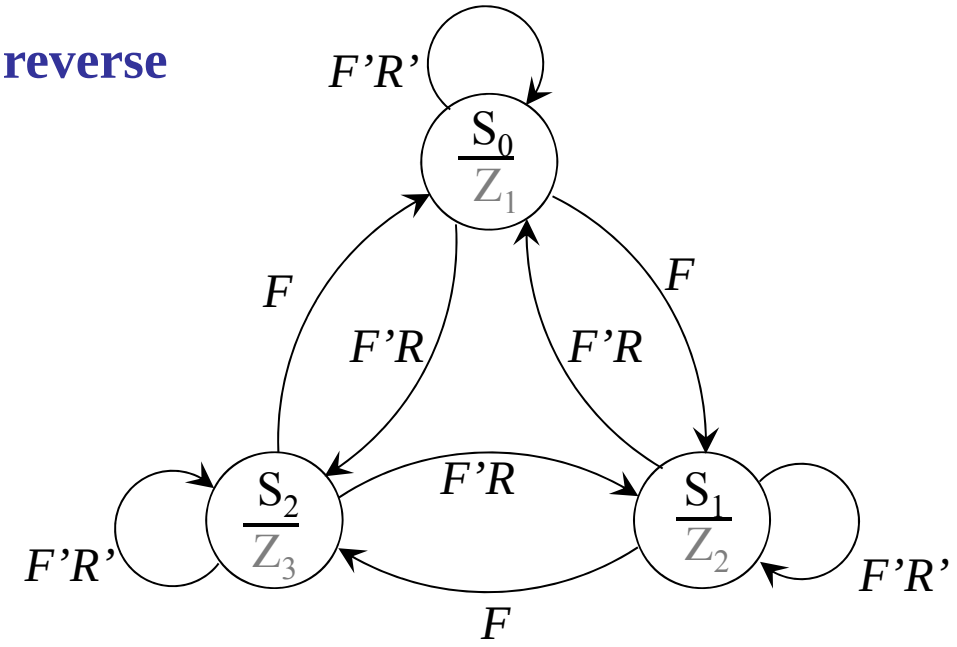
Alphanumeric State Graph Notation (1/2)

- When a sequential circuit has several inputs
  - Label the state graph arcs with alphanumeric input variable

F = forward **R = reverse**



(a)



(b)

not complete

PS	NS				Output		
	FR = 00	01	10	11	Z_1	Z_2	Z_3
S_0	S_0	S_2	S_1	S_1	1	0	0
S_1	S_1	S_0	S_2	S_2	0	1	0
S_2	S_2	S_1	S_0	S_0	0	0	1

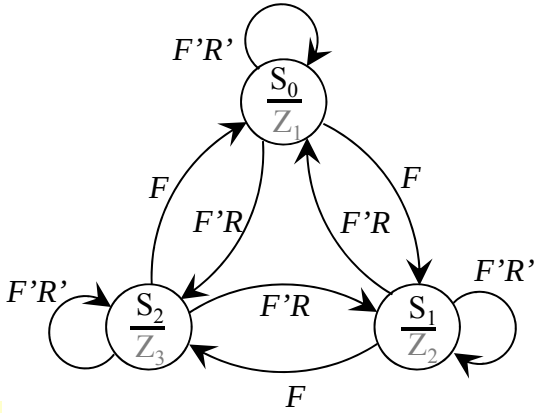
Alphanumeric State Graph Notation (2/2)

- **Property of the completely specified state graph**
  - **OR** together all input labels on arcs emanating from a state, the result can be reduced to 1

$$F + F'R + F'R' = F + F' = 1$$

  - **AND** together any pair of input labels on arcs emanating from a state, the result can be reduced to 0

$$F \cdot F'R = 0, \quad F \cdot F'R' = 0, \quad F'R \cdot F'R' = 0$$



- For large sequential circuits (4 inputs, 4 outputs)
  - X_1X_4'/Z_2Z_3 1--0/0110
  - $-/Z_1$ for any combination of input values, the indicated state will occur and output Z_1=1